ABSTRACT OF THE DISCLOSURE

A plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, an invalid address detecting circuit, and an invalid signal outputting circuit are comprised. Upon command input, the invalid address detecting circuit invalidates a command in the case where the invalid address detecting circuit detects a fact that an address signal supplied from exterior indicates an invalid address space. Therefore, at the time of invalid address supply, internal circuits are not activated and an erroneous write or erase operation can be prevented. Since the internal circuits do not operate, power consumption can be reduced substantially. The invalid signal outputting circuit outputs an invalid signal by receiving the fact of invalid address signal detection by the invalid address detecting circuit. Therefore, a system unit mounting the semiconductor memory device can easily recognize that the invalid address signal has been supplied to the semiconductor memory device. As a result, a malfunctioning can be prevented and reliability of the system unit improves.